L Number	Hits	Search Text	DB	Time stamp
3	50	((((((layout same wir$4 same connect$5) and 716/$.ccls.) and dimension$4) and place$5) and pair) and rout$5) and pin and netlist	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/15 08:01
4	22	(wir$4 same connectivity) and 716/$.ccls. and dimension$4 and place$5 and pair and rout$5 and pin and netlist	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/15 08:02
-	6417	layout same wir$4 same connect$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/12 16:08
-	655	(layout same wir$4 same connect$5) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/12 15:13
-	0	((layout same wir$4 same connect$5) and 716/$.ccls.) and demension	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/12 15:14
-	296	((layout same wir$4 same connect$5) and 716/$.ccls.) and dimension$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/12 15:14
-	258	(((layout same wir$4 same connect$5) and 716/$.ccls.) and dimension$4) and place$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/12 15:15
-	147	((((layout same wir$4 same connect$5) and 716/$.ccls.) and dimension$4) and place$5) and pair	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/12 15:15
-	131	(((((layout same wir$4 same connect$5) and 716/$.ccls.) and dimension$4) and place$5) and pair) and rout$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/12 17:00
-	93	((((((layout same wir$4 same connect$5) and 716/$.ccls.) and dimension$4) and place$5) and pair) and rout$5) and pin	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/15 07:39

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1	US 20030188274 A1	20031002	17	Floor plan tester for integrated circuit design	716/4
2	US 20030121019 A1	20030626	14	Tool suite for the rapid development of advanced standard cell libraries	716/12
3	US 20030115564 A1	20030619	80	Block based design methodology	716/8
4	US 20030079197 A1	20030424	18	Method and apparatus to generate a wiring harness layout	716/13
5	US 20030009727 A1	20030109	90	Circuit designing apparatus, circuit designing method and timing distribution apparatus	716/1
6	US 20020166098 A1	20021107	80	Block based design methodology	716/1
7	US 20020083398 A1	20020627	90	Circuit designing apparatus, circuit designing method and timing distribution apparatus	716/1
8	US 20020073380 A1	20020613	89	Block based design methodology with programmable components	716/1
9	US 20020016952 A1	20020207	81	Block based design methodology	716/18
10	US 20010042237 A1	20011115	80	Block based design methodology	716/8
11	US 20010039641 A1	20011108	80	Block based design methodology	716/8
12	US 20010025369 A1	20010927	78	Block based design methodology	716/18
13	US 20010018756 A1	20010830	81	Block based design methodology	716/1
14	US 20010016933 A1	20010823	80	Block based design methodology	716/1
15	US 20010010090 A1	20010726	22	Method for design optimization using logical and physical information	716/2

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16	US 6651225 B1	20031118	179	Dynamic evaluation logic system and method	716/4
17	US 6631470 B2	20031007	71	Block based design methodology	716/3
18	US 6629293 B2	20030930	65	Block based design methodology	716/4
19	US 6618834 B2	20030909	88	Circuit designing apparatus, circuit designing method and timing distribution apparatus	716/2
20	US 6594800 B2	20030715	71	Block based design methodology	716/1
21	US 6574778 B2	20030603	70	Block based design methodology	716/1
22	US 6567957 B1	20030520	71	Block based design methodology	716/4
23	US 6557145 B2	20030429	20	Method for design optimization using logical and physical information	716/2
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26	US 6539533 B1	20030325	14	Tool suite for the rapid development of advanced standard cell libraries	716/17
27	US 6477695 B1	20021105	14	Methods for designing standard cell transistor structures	716/17
28	US 6457157 B1	20020924	19	I/O device layout during integrated circuit design	716/2
29	US 6449761 B1	20020910	37	Method and apparatus for providing multiple electronic design solutions	716/11
30	US 6446239 B1	20020903	38	Method and apparatus for optimizing electronic design	716/2

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31	US 6389379 B1	20020514	157	Converification system and method	703/14
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33	US 6345379 B1	20020205	59	Method and apparatus for estimating internal power consumption of an electronic circuit represented as netlist	716/4
34	US 6338972 B1	20020115	18	Off-grid metal layer utilization	438/14
35	US 6324675 B1	20011127	32	Efficient iterative, gridless, cost-based fine router for computer controlled integrated circuit design	716/13
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38	US 6175947 B1	20010116	18	Method of extracting 3-D capacitance and inductance parasitics in sub-micron VLSI chip designs using pattern recognition and parameterization	716/5
39	US 6088519 A	20000711	16	Method and system for improving a placement of cells using energetic placement with alternating contraction and expansion operations	716/9
40	US 6075932 A	20000613	56	Method and apparatus for estimating internal power consumption of an electronic circuit represented as netlist	716/4
41	US 5987086 A	19991116	113	Automatic layout standard cell routing	716/1
42	US 5841664 A	19981124	12	Method for optimizing track assignment in a grid-based channel router	716/14

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43	US 5822214 A	19981013	135	CAD for hexagonal architecture	716/10
44	US 5818729 A	19981006	23	Method and system for placing cells using quadratic placement and a spanning tree model	716/9
45	US 5754444 A	19980519	17	Method and system for improving a placement of cells using energetic placement units alternating contraction and expansion operations	716/9
46	US 5696694 A	19971209	84	Method and apparatus for estimating internal power consumption of an electronic circuit represented as netlist	716/5
47	US 5682320 A	19971028	83	Method for electronic memory management during estimation of average power consumption of an electronic circuit	716/4
48	US 5666289 A	19970909	13	Flexible design system	716/8
49	US 5568636 A	19961022	18	Method and system for improving a placement of cells using energetic placement with alternating contraction and expansion operations	716/9
50	US 5311443 A	19940510	8	Rule based floorplanner	716/10